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APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Kwan-Ju Koh**, a citizen of Korea, residing at 407-101, Keumkang Maeul, Jung 4-dong, Wonmi-Ku, Bucheon-city, Kyungki-do 420-429, Korea have invented a new and useful **SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME**, of which the following is a specification.

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to a semiconductor device having a multi-layered metal wire structure and, more particularly, to a semiconductor device having an interlayer insulation film with a low capacitance and a method of fabricating the same.

BACKGROUND

[0002] With the trend toward more highly integrated, multi-layer semiconductor devices, the use of multi-layered wiring techniques has been proposed as one of the important techniques for implementing such highly integrated, multi-layer semiconductor devices. Multi-layer wiring techniques typically use metal wire layers and insulation layers that are alternately formed on a top surface of a semiconductor substrate on which circuit devices are formed. In addition, such multi-layer wiring techniques utilize a circuit operation that is performed by electrically connecting the metal wire layers, which are separated by the insulation layers, through via holes.

[0003] However, in such a multi-layered metal wire structure the space between the metal wires narrows as the level of integration of the semiconductor device increases. As a result, the effects of parasite resistance or parasite capacitance between adjacent metal wires in the same layer or between lower and upper metal wire layers becomes more significant.

[0004] As is known, parasitic resistance or capacitance deteriorates an electrical characteristic due to a delay induced by an RC (resistance and capacitance), disturbs or limits the high speed operation of the semiconductor device, and typically increases power consumption and signal leakage of the semiconductor device.

[0005] Accordingly, to reduce the parasitic capacitance, studies for materials having a low dielectric constant K, for example, a SiC family among oxide materials of an existing TEOS (tetra ethyl ortho silicate) family has been progressed actively. However, in the case that new materials with such a low dielectric constant are used, additional equipment must be used and a process parameter optimization of each unit process for the new materials, thereby increasing processing costs.

[0006] Accordingly, methods of reducing the parasitic capacitance while using the oxide materials of the existing TEOS family as they are have been studied. As a result, there have been proposed methods where air gaps are formed in an interlayer insulation film between adjacent metal wires in order to reduce an overall capacitance, the so called "air gap formation method at intralevel." Techniques related to this are disclosed in U.S. Patent Nos. 6,472,719, 6,423,630, 6,403,461, 6,376,330, 6,358,845, and 6,268,276.

[0007] Fig. 1 is a sectional view of a multi-layered metal wire structure where air gaps are formed at an intralevel using a known technique. As shown in Fig. 1, lower metal wire layers 102 are formed on a structure of a semiconductor substrate, upper metal wire layers 106 are formed above the lower metal wire layers 102 via an interlayer insulation film 104, and the upper and lower metal wire layers 106 and 102 are electrically connected to each other through via holes 108. In addition, air gaps 110 are formed in the interlayer insulation film 104 between the lower metal wire layers 102.

[0008] However, conventionally, as shown in Fig. 1, the air gaps 110 are formed in only intralevels between the lower metal wire layers 102. That is, because it is impossible to form the air gaps between the lower metal wire layers 102 and the upper metal wire layers 106, there is a limit on the reduction of an overall capacitance.

[0009] Accordingly, if air gaps can be formed between the lower metal wire layers 102 and the upper metal wire layers 106, the overall capacitance can be significantly reduced. As a result, there is a strong need for the formation of air gaps at such an interlevel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1 is a sectional view of a multi-layered metal wire structure where air gaps are formed at an intralevel using a known method.

[0011] Fig. 2 is a sectional view of an example multi-layered metal wire structure in which air gaps are formed at an interlevel.

[0012] Figs. 3A to 3I are views showing an example method of forming the air gaps of Fig. 2.

DETAILED DESCRIPTION

[0013] As described in greater detail below, an example semiconductor device having a multi-layered metal wire structure includes first and second interlayer insulation films provided between lower metal wire layers and upper metal wire layers. In addition, air gaps may be formed in the first interlayer insulation film at an interlevel between the upper and lower metal wire layers and via holes may connect the upper and lower metal wire layers.

[0014] Still further, an example method of fabricating a semiconductor device described in greater detail below may form a first interlayer insulation film above a lower insulation film on a top surface of a semiconductor substrate where an individual element including lower metal wire layers is formed. The example method may form a first mask film and a second mask film on the first interlayer insulation film sequentially and may form a first etch mask to be used to form air gaps by selectively etching the second mask film. Still further, the example method may

deposit a third mask film on the first etch mask and the first mask film and may form a second etch mask by etching the third mask film and exposed the first mask film. The second etch mask may be made from the third mask film remaining on side walls of the first etch mask and the first mask film remaining below the first etch mask and the third mask film. Still further, the example method may remove the first etch mask and substantially simultaneously form open pores in the first interlayer insulation film by etching the first etch mask and exposed the first interlayer insulator film using the second etch mask. The example method may also form air gaps consisting of closed pores in the first interlayer film at an interlevel between upper metal wire layers and the lower metal wire layers by forming a second interlayer insulation film after removing the second etch mask and may form via holes to expose the lower metal wire layers by selectively removing the first and second interlayer insulation films, filling metal material in the via holes, and then forming the upper metal wire layers.

[0015] Fig. 2 is a sectional view of an example multi-layered metal wire structure where air gaps are formed at an interlevel. Figs. 3a to 3i are views showing an example process of forming the air gaps of Fig. 2. As shown in the figures, an interlayer insulation film 16 consisting of first and second interlayer insulation films is formed above a lower insulation film 14 on a top surface of a semiconductor substrate where an individual element including lower metal wire layers 12 is formed. In addition, via holes 20 for connecting upper metal wire layers 18 and the lower metal wire layers 12 are formed in the interlayer insulation film 16.

[0016] In the example semiconductor device shown in Fig. 2, air gaps 22 are formed in the interlayer insulation film 16 at an interlevel between the upper and lower metal wire layers 18 and 12. This allows the reduction of an overall

capacitance over the conventional semiconductor devices where air gaps are formed in the interlayer insulation film at the intralevel between the lower metal wire layers.

[0017] Now turning to the example method of Fig. 3, Fig. 3A illustrates that the first interlayer insulation film 16a is formed above the lower insulation film 14 on a top surface of a semiconductor substrate where an individual element including lower metal wire layers 12 is formed. An oxide film which is formed by a deposition of materials of commonly used TEOS family can be used as used in the first interlayer insulation film 16.

[0018] Subsequently, as shown in Fig. 3B, a nitride film 24 and an oxide film 26 are formed on the first interlayer insulation film 16a sequentially, and then, as shown in Fig. 3C, by applying, exposing and developing a photosensitive film on the oxide film 26, a pattern of mask 28 for exposing a portion of the oxide film 26 corresponding to a position where air gaps are to be formed is formed. At this time, the position where air gaps are to be formed is preferably a top portion between the lower metal wire layers 12, not a top portion of the metal wire layers where via holes 20 are to be formed.

[0019] Next, as shown in Fig. 3D, after forming a pattern of oxide film 26' by etching the oxide film 26 exposed using the pattern of mask 28 as a mask, the pattern of mask 28 is removed, and then a cleaning process is performed.

[0020] Next, as shown in Fig. 3E, a nitride film 30 is deposited on the pattern of oxide film 26', and then, as shown in Fig. 3F, by etching the nitride film 30 above the pattern of oxide film 26' and the nitride film 24 exposed below the pattern of oxide film 26', side walls 30' are formed in the pattern of oxide film 26', and simultaneously a pattern of nitride film 24' is formed.

[0021] Continuously, as shown in Fig. 3G, the first interlayer insulation film 16a is etched by using a dry isotropic etching. By the dry isotropic etching, the first interlayer insulation film 16a is etched into a shape close to a circle, and accordingly, open pores 22' are formed in the first interlayer insulation film 16a. At this time, a specific shape, e.g., a size and an extent of opening, of the open pores 22' formed by the isotropic etching can be adjusted by using etching time, for example.

[0022] In addition, the pattern of oxide film 26' is also removed when the first interlayer insulation film 16a is etched.

[0023] Next, as shown in Fig. 3H, the nitride film 24' and the side walls 30' remaining on the first interlayer insulation film 16a are removed, and then, as shown in Fig. 3I, after forming a second interlayer insulation film 16b by successively depositing a TEOS oxide film made from the same material as the first interlayer insulation film 16a on the first interlayer insulation film 16a, a top surface of the second interlayer insulation film 16b is planarized by means of a chemical and mechanical polishing process.

[0024] At this time, the second interlayer insulation film 16b is deposited on the first interlayer insulation film 16a such that openings of open pores 22' are blocked and, as a result, closed pores 22 are formed in the first interlayer insulation film 16a.

[0025] Accordingly, the closed pores 22 formed in the first interlayer insulation film 16a function as air gaps in terms of a dielectric constant of an insulator.

[0026] Finally, to complete the formation of the multi-layered metal wire structure as shown in Fig. 2, via holes 20 to expose the lower metal wire layers 12 are formed by selectively etching the second 16b and first 16a interlayer insulation films, the via holes 20 are filled with metal material, and then upper metal wire layers are formed.

[0027] As apparent from the above description, in the example semiconductor device having the multi-layered metal wire structure described herein, because air gaps are formed at the interlevel between the lower metal wire layers and the upper metal wire layers, sizes of air gaps can be significantly increased over the prior art where air gaps are formed between metal wires at the same layer. Accordingly, since a capacitance can be significantly reduced, an insulation characteristic of an interlayer insulation film can be improved.

[0028] In addition, since a parasitic capacitance can be significantly reduced while using existing interlayer insulation material as it is, a high speed operation device can be realized at an inexpensive process cost.

[0029] Although certain methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. To the contrary, this patent covers all embodiments fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.